REMARKS

Claims 1-28 are pending in the present application. Claims 1, 4, 8, 9, 13, 16-21 and 24-28 have been amended.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on July 6, 2001.

Priority Under 35 U.S.C. 119

Enclosed is a copy of a Claim of Priority Letter dated July 6, 2001, filed along with the present application. Also enclosed is a dated, stamped postcard receipt provided as evidence that the Claim of Priority Letter was received by the U.S. Patent office. **The Examiner is respectfully requested to acknowledge receipt of the certified copy of the priority document, and to confirm that the Claim for Priority under 35 U.S.C. 119 is complete in the present application.**

Claim Rejections-35 U.S.C. 102

Claims 1, 2, 17 and 18 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Lu et al. reference (U.S. Patent No. 6,165,276). This rejection is respectfully traversed for the following reasons.

The semiconductor manufacturing apparatus of claim 1 includes in combination

a wafer support "that has a tapered lateral side that supports an edge of a wafer from below said wafer"; a stage on which said wafer is placed; and wafer clamps "that come into contact with a perimeter of said wafer from above said wafer". Applicant respectfully submits that the Lu et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has alleged that bottom electrode 15 as illustrated in Fig. 1 of the Lu et al. reference may be interpreted as the wafer support of claim 1. However, bottom electrode 15 as illustrated in Fig. 1 of the Lu et al. reference does not have a tapered lateral side that supports an edge of a wafer from below the wafer, as alleged by the Examiner. One of ordinary skill would readily understand that by definition, the lateral side of bottom electrode 15 would correspond to **the side wall** of bottom electrode 15. As may be readily understood in view of Fig. 1 of the Lu et al. reference, wafer 25 is placed on and supported by a top surface of bottom electrode 15, not a tapered lateral side thereof. Particularly, the lateral sides of bottom electrode 15 do not support an edge of wafer 25 from below the wafer. That is, only a central portion of the upper surface of bottom electrode 15 is illustrated as in contact with a central portion of wafer 25, whereby edges of wafer 25 are not supported or in contact with bottom electrode 15. The Lu et al. reference thus fails to meet the features of claim 1. Applicant therefore respectfully submits that the semiconductor manufacturing apparatus of claim 1 distinguishes over the Lu et al. reference as relied upon by the Examiner, and that this rejection of claims 1 and 2 is improper for at least these

reasons.

The wafer-securing method of claim 17 includes in combination "disposing a stage that has an upper surface on which a wafer is to be placed, and a wafer support that has a tapered lateral side that supports an edge of said wafer from below said wafer", and "placing said wafer on said stage and determining a position at which said wafer is to be placed by said edge of said wafer coming into contact with said lateral side".

Applicant respectfully submits that since the Lu et al. reference as relied upon by the Examiner does not include a wafer support having a tapered lateral side that supports an edge of a wafer from below the wafer, the Lu et al. reference clearly fails to meet the features of claim 17. That is, since the Lu et al. reference does not dispose a stage including a wafer support that has a tapered lateral side that supports an edge of a wafer from below the wafer, the Lu et al. reference clearly fails to disclose placing the wafer on the stage and determining a position at which the wafer is to be placed by the edge of the wafer coming into contact with the lateral side of the wafer support. Accordingly, Applicant respectfully submits that the wafer-securing method of claim 17 distinguishes over the Lu et al. reference as relied upon by the Examiner, and that this rejection of claims 17 and 18 is improper for at least these reasons.

Claims 1-7, 9-12 and 17-23 have been rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's prior art. This rejection is respectfully traversed for the following reasons.

As emphasized previously, the semiconductor manufacturing apparatus of claim 1 includes in combination a wafer support "that has a tapered lateral side that supports an edge of a wafer from below said wafer". The Examiner has alleged that Applicant's admitted prior art includes wafer support 10 as illustrated in Fig. 6 which meets these features of claim 1. However, tapered recess 10a as illustrated in Fig. 6 of Applicant's admitted prior art **does not support an edge of wafer 14 from below the wafer**. Applicant therefore respectfully submits that the semiconductor manufacturing apparatus of claim 1 distinguishes over the Lu et al. reference as relied upon by the Examiner, and that this rejection of claims 1-7 and 9-12 is improper for at least these reasons.

Applicant also respectfully submits that since tapered recess 10a in Fig. 6 of Applicant's admitted prior art does not support wafer 14 from below the wafer, Applicant's admitted prior art clearly fails to disclose placing a wafer on a stage and determining a position at which said wafer is to be placed by the edge of the wafer coming into contact with a lateral side of a wafer support, whereby the tapered lateral side supports an edge of the wafer from below the wafer, as featured in claim 17. Applicant therefore respectfully submits that the wafer-securing method of claim 17 distinguishes over Applicant's admitted prior art as relied upon by the Examiner, and that this rejection of claims 17-23 is improper for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 8 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. However, Applicant respectfully submits that claims 8 and 24 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner at least by virtue of dependency upon claims 1 and 17 respectively, for the reasons as set forth above.

Applicant also respectfully notes the Examiner's acknowledgment that claims 13-16 and 25-28 are allowed. In view of this acknowledgment, claim 25 has been amended to be in independent form.

Conclusion

Applicant respectfully notes that claim 25 has been amended merely to be in independent form as including the features of dependent claim 17, not to further distinguish over the prior art as relied upon by the Examiner. This should be particularly clear in view of the Examiner's acknowledgment of allowable subject matter. Also, the remaining claims have been variously amended merely to improve form, not to further distinguish over the prior art as relied upon by the Examiner. Accordingly, the corresponding amendments to the claims should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the

rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

Andrew J. Telesz, Jr.
Registration No. 33,581

AJT:dmc

VOLENTINE FRANCOS, P.L.L.C.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: Copy of Claim of Priority Letter
Copy of postcard receipt